REMARKS

Claims 1-65 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 102(e) Rejection:

The Examiner rejected claims 1, 2, 4, 5, 13-19, 21-23, 30, 33-44, 49-51 and 56-65 under 35 U.S.C. § 102(e) as being anticipated by Chen, et al. (U.S. Patent 6,763,365) (hereinafter "Chen"). Applicants traverse this rejection for at least the following reasons.

Regarding claim 1, contrary to the Examiner's assertion, Chen fails to disclose *in response to executing a single arithmetic instruction, multiplying a first number by a second number; and adding implicitly a partial result from a previously executed single arithmetic instruction to generate a result that represents the first number multiplied by the second number summed with the partial result, wherein the partial result comprises a high order portion of a result of the previously executed single arithmetic instruction.* The Examiner's submits that this entire collection of limitations is taught in col. 11, lines 34-40 (noting only, "feedback; first using circuit; then using circuit again with register provided with output from first operational stage"), and col. 10, lines 13-26 (noting only, "multiple-accumulate instruction; first addend comes from the rightmost k bits of Z register; bits are added to the k bits in the rightmost portion of the product A, B").

Applicants assert that the Examiner has failed to fully and clearly state his ground of rejection of claim 1 and has therefore failed to establish a *prima facie* case of anticipation given that the burden of proof falls on the Office. The Examiner's remarks (quoted above) refer only generally to features that he believes are taught by the cited passages of Chen without describing how he believes these passages (or elements described therein) disclose each of the above-referenced limitations of claim 1. Since the features noted by the Examiner do not correspond to the language recited in the above-referenced claim limitations, it is not clear or how he interprets the cited passages to teach

the specific limitations of claim 1 as arranged in the claim. The statute clearly places the burden of proof on the Patent Office to prove a *prima facie* rejection. *In re Warner*, 154 USPQ 173, 177 (C.C.P.A. 1967), *cert. denied*, 389 U.S. 1057 (1968). The Examiner's vague assertions, which lack a clear mapping between the teachings of Chen and Applicants' claim, cannot be said to establish a *prima facie* case of anticipation.

In addition, Applicants assert that the cited passages do not disclose the above-referenced limitations. For example, nothing in the cited passages describes *in response to executing a single arithmetic instruction, multiplying a first number by a second number; and adding implicitly a partial result from a previously executed single arithmetic instruction*, as recited in claim 1. The "multiplication with feedback" described therein appears to refer to a single multiplication instruction. For example, the cited passage in col. 11 describes the multiplication operation "AB mod N." In Chen, a hardware circuit may execute this single multiplication operation in two phases. **However, there is no feedback of a partial result from a previously executed single arithmetic instruction (i.e., a different instruction) described.** The Examiner's citation in col. 10 describes the operation of Chen's hardware circuit in more detail, but also does not disclose feedback of a partial result from a previously executed single arithmetic instruction, as required by Applicants' claim.

Further regarding claim 1, Chen fails to disclose *storing at least a portion of the generated result; and using the stored at least a portion of the generated result in a subsequent computation in the cryptography application*. The Examiner's submits that these limitations are taught in col. 4, lines 8-11 (noting only, "multiplication and addition are performed by large circuits"); in col. 10, lines 13-36 (without including any remarks regarding this passage); and in col. 11, lines 34-40 (noting only, "feedback; first using circuit; then using circuit again with register provided with output from first operational stage (multiplication with feedback)"). The Examiner has again failed to explain how he believes the cited passages teach the above-referenced limitations. Applicants assert that since they have nothing to do with storing a portion of the generated result (i.e., the result of the multiplying and adding recited in claim 1), nor with using the stored portion in a

subsequent computation in a cryptography application, they clearly do not disclose the above-referenced limitations of claim 1. Instead, this passage again appears to describe the execution of a single multiplication instruction.

As discussed above, the descriptions of individual features listed by the Examiner do not teach the specific combination of limitations recited in claim 1, as arranged in the claim. The Examiner is clearly attempting a piecemeal reconstruction of Applicants' invention in hindsight without consider the claimed invention as a whole. Such reconstruction is improper. *See, e.g., Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). For example, a general reference to "multiplication with feedback" and a description of a hardware circuit usable to execute a single multiplication instruction clearly do not teach the specific limitations recited in claim 1 regarding *multiplying a first number by a second number; and adding implicitly a partial result from a previously executed single arithmetic instruction*. In another example, the Examiner's statement that "multiplication and addition are performed by large circuits" teaches nothing about the limitations recited in claim 1.

Anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, **arranged as in the claim**. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The **identical invention must** be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As discussed above, Chen clearly fails to disclose the actions performed in response to a single arithmetic instruction as recited in Applicants' claim 1.

For at least the reasons above, Chen cannot be said to anticipate claim 1 and removal of the rejection there is respectfully requested.

Independent claims 43, 57, and 64 include limitations similar to those recited in claim 1 and discussed above, and were rejected for similar reasons. Therefore, the arguments presented above apply with equal force to these claims, as well.

Independent claim 18 includes limitations similar to those recited in claim 1 and discussed above, and was rejected for reasons similar to those discussed above regarding claim 1. In fact, the Examiner includes several of the same citations and notes several of the same features of Chen in rejecting claim 18. Therefore, Applicants traverse this rejection for at least the reasons presented above regarding limitations in this claim that are similar to those in claim 1.

In addition, claim 18 recites *adding a third number to generate a result that represents the first number multiplied by the second number summed with the partial result and the third number.* Applicants note that the Examiner does not include any additional remarks regarding this limitation or any additional citations in the reference to teach it. **Therefore, the Examiner has failed to state a *prima facie* rejection of claim 18.** Applicants assert that the Examiner's citations and remarks regarding "multiplication and addition are performed by large circuits," "multiplication with feedback," and "arithmetic operations to support acceleration of cryptographic functions" teach nothing about a single arithmetic instruction that results in the operations recited in claim 18.

For at least the reasons above, Chen cannot be said to anticipate claim 18 and removal of the rejection thereof is respectfully requested.

Claims 50, 61, and 65 include limitations similar to those recited in claims 1 and 18 and discussed above, and were rejected for the same reasons as claims 1 and 18. Therefore, the arguments presented above apply with equal force to these claims, as well.

Section 103(a) Rejection:

The Examiner rejected claims 3, 20, 45 and 52 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Lasher, et al. (U.S. Patent 4,863,247) (hereinafter "Lasher"), claims 6-12, 24-29, 31, 32, 47, 48, 53, 54 and 55 as being unpatentable over

Chen in view of Stribaek, et al. (U.S. Patent 7,181,484) (hereinafter "Stribaek"), claim 17 as being unpatentable over Chen in view of Chen, et al. (U.S. Patent 6,687,725) (hereinafter "Chen2"), claims 46 and 47 as being unpatentable over Chen-Stribaek and further in view of Lasher.

In regard to the rejections under both § 102(e) and § 103(a), Applicants assert that numerous ones of the dependent claims recite further distinctions over the cited art. Applicants traverse the rejection of these claims for at least the reasons given above in regard to the claims from which they depend. However, since the rejections have been shown to be unsupported for the independent claims, a discussion of the dependent claims is not necessary at this time. Applicants reserve the right to present additional arguments.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/60000-32301/RCK.

Respectfully submitted,

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